ABSTRACT OF THE DISCLOSURE

A memory test circuit includes a collar for coupling to a memory device for switching an address bus and a data bus of the memory device between an external circuit and the collar in response to a switching signal; and a controller coupled to the collar for generating the switching signal, a test vector, and control signals between the controller and the collar on as few as seven control lines for testing the memory device with the test vector. Multiple memory devices of various sizes may be tested with the same controller concurrently.